In the Claims

This listing of all claims will replace all prior versions, and listings, of claims in the application:

1-17. Canceled.

18. (original) A method of forming a replacement gate structure for CMOS devices on a semiconductor wafer, comprising:

providing a patterned gate structure having a sacrificial gate dielectric, sidewall spacers, shallow trench isolation, source and drain ion implantation regions, and a polysilicon layer over said gate dielectric;

depositing a Si_3N_4 / SiO_2 bilayer surrounding the gate region;

removing said polysilicon layer and sacrificial gate dielectric;

growing said gate dielectric over said patterned gate structure;

depositing a metal gate liner over said gate dielectric;

depositing a silicon layer over said metal liner;

planarizing structure using chemical mechanical polishing (CMP);

forming a silicide metal layer;

annealing said gate structure; and

removing any unreacted metal.

19. (original) The method of claim 18 further comprising depositing a silicide barrier liner over said metal gate liner, and depositing a silicon gate fill over said barrier.

20. Canceled.